Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Currently amended): A circuit interconnect comprising:

a substrate having a fold at a first end of the interconnect; and

a conductor layer supported by the substrate, the conductor layer comprising a high frequency transmission line, and a pad array of a grid array interface adjacent to the first end, the transmission line being connected to a pad of the pad array,

wherein the fold is between a first portion and a second portion of the interconnect such that the first portion is essentially parallel to the second portion along a length of the interconnect extending away from the fold, and

wherein the interconnect connects distinct circuit elements together without essentially vertically stacking the elements for interconnection.

Claim 2 (Original): The circuit interconnect of Claim 1, wherein a material of the substrate is selected from a flexible or pliable material, a rigid material and a semi-rigid material that is foldable.

Claim 3 (Original): The circuit interconnect of Claim 1, wherein the pad array is an array of interconnection pads, the pad array being a portion of the grid array interface, the grid array interface being selected from a ball grid array and a pin grid array.

Claim 4 (Original): The circuit interconnect of Claim 1, further comprising:

a stiffener that supports the substrate, the stiffener being between the first portion and the second portion adjacent to a surface of the substrate opposite to a surface that supports the transmission line and the pad array.

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Claim 5 (Original): The circuit interconnect of Claim 1, further comprising a bend in the first portion and the second portion that changes an orientation of the first end relative to a second end of the interconnect that is opposite to the first end.

Claim 6 (Original): The circuit interconnect of Claim 1, wherein the conductor layer further comprises:

an electrical interface adjacent to a second end of the interconnect, the second end being opposite to the first end, the electrical interface being connected to the transmission line.

Claim 7 (Original): The circuit interconnect of Claim 6, wherein the pad array and electrical interface are adjacent to a surface of the substrate exterior to a space between the parallel first and second portions, the pad array being in the first portion and the electrical interface being in one or both of the first portion and the second portion.

Claim 8 (Original): The circuit interconnect of Claim 7, further comprising another conductor layer supported by a surface of the substrate interior to the space between the parallel first and second portions.

Claim 9 (Original): The circuit interconnect of Claim 7, wherein the electrical interface is one or more of a portion of a grid array interface selected from ball grid array and a pin grid array, a dual in-line array and a four-sided or rectangular edge array.

Claim 10 (Original): The circuit interconnect of Claim 7, further comprising a bend that changes an orientation plane of one of the electrical interface adjacent to the second end and the pad array adjacent to the first end relative to the other.

Claim 11 (Currently amended): The circuit interconnect of Claim 7, wherein ~~the interconnect connects distinct circuit elements together without essentially vertically stacking the elements for interconnection,~~ the pad array ~~connecting~~ connects to a first circuit element adjacent to the first end of the interconnect, the electrical interface

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connecting to a second circuit element adjacent the second end of the interconnect, the distinct circuit elements being a distance apart about equal to or less than the length of the circuit interconnect.

Claim 12 (Original): The circuit interconnect of Claim 1, wherein the substrate has another fold at a second end of the interconnect, the second end being opposite the first end, such that the first portion and the second portion are between the folds, the substrate essentially forming a loop.

Claim 13 (Currently amended): A folded flex circuit interconnect comprising:

a flexible substrate having a first fold at a first end of the interconnect and second fold at a second end of the interconnect opposite the first end; and

a conductor layer supported by the substrate, the conductor layer comprising one or more electrical traces and a pad array of a grid array interface, the pad array being adjacent to the first end and connected to one or more of the electrical traces,

wherein a first portion and a second portion of the interconnect are between the first fold and the second fold such that the first portion is essentially parallel to the second portion and the substrate essentially forms a loop, and

wherein the folded flex circuit interconnect connects distinct circuit elements together without vertically stacking the elements for interconnection.

Claim 14 (Original): The flex circuit interconnect of Claim 13, wherein one or more of the electrical traces is a transmission line that supports one or both of microwave and millimeter wave signal propagation.

Claim 15 (Original): The folded flex circuit interconnect of Claim 13, further comprising a bend that changes an orientation plane of one of the first end and the second end relative to the other.

Claim 16 (Original): The folded flex circuit interconnect of Claim 13, wherein the substrate and conductor layer are fabricated as an essentially planar structure having two separate termination ends, the structure being subsequently

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folded such that the two separate termination ends are brought together in proximity to one another to form the interconnect.

Claim 17 (Original): The folded flex circuit interconnect of Claim 13, wherein the conductor layer further comprises:

an electrical interface adjacent to the second end of the interconnect, the electrical interface being connected to one or more of the electrical traces.

Claim 18 (Original): The folded flex circuit interconnect of Claim 17, wherein the pad array and electrical interface are adjacent to a surface of the substrate exterior to a space between the parallel first and second portions, the pad array being in the first portion and the electrical interface being in one or both of the first portion and the second portion.

Claim 19 (Original): The folded flex circuit interconnect of Claim 17, wherein the grid array interface is selected from a ball grid array and a pin grid array, and wherein the electrical interface is one or more of a portion of another grid array interface selected from ball grid array and a pin grid array, a dual in-line array and a four-sided or rectangular edge array.

Claim 20 (Cancelled).

Claim 21 (Original): The folded flex circuit interconnect of Claim 17, wherein the conductor layer further comprises:

another electrical interface between the first end and the second end of the interconnect, the other electrical interface being connected to one or more of the electrical traces.

Claim 22 (Original): An optics module comprising:

an optical unit; and

a folded flex circuit interconnect having a first portion and a second portion between a first fold at a first end of the interconnect and a second fold at a second end

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of the interconnect opposite the first end, the first portion being essentially parallel to the second portion along a length of the interconnect,

wherein the folded flex circuit interconnect connects the optical unit to a motherboard without vertically stacking the optical unit and the motherboard together for such interconnection.

Claim 23 (Original): The optics module of Claim 22, wherein the folded flex circuit interconnect carries high frequency signals between the interconnected motherboard and optical unit, the high frequency signals being one or both of microwave and millimeter wave frequency signals.

Claim 24 (Original): The optics module of Claim 22, wherein the optical unit is one of an optical transmitter, an optical receiver, and an optical transceiver.

Claim 25 (Original): The optics module of Claim 22, wherein the folded flex circuit interconnect comprises a pad array of a grid array interface located in the first portion adjacent to the first fold, and an electrical interface located in one or both of the first portion and the second portion adjacent to the second fold, the pad array connecting to the motherboard, the electrical interface connecting to the optical unit.

Claim 26 (Original): The optics module of Claim 25, wherein the folded flex circuit interconnect further comprises a conductor layer comprising an electrical trace, the electrical trace connecting the pad array to the electrical interface.

Claim 27 (Original): The optics module of Claim 26, wherein the electrical trace comprises a high frequency transmission line selected from a microstrip transmission line, a coplanar waveguide, a stripline transmission line, and a fin line transmission line.

Claim 28 (Original): The optics module of Claim 25, wherein the grid array interface is selected from a ball grid array and a pin grid array, the electrical interface being one of a portion of a grid array interface selected from a ball grid array and a pin grid array, a rectangular edge array and a dual in-line array.

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Claim 29 (Original): The optics module of Claim 25, wherein the folded flex circuit interconnect further comprises another electrical interface located in one of the first portion and the second portion between the first fold and the second fold, the other electrical interface connecting to an electrical component.

Claim 30 (Original): The optics module of Claim 22, wherein the folded flex circuit interconnect comprises:

a conductor layer supported by a substrate, the conductor layer comprising an electrical trace;

a pad array of a grid array interface supported by the substrate adjacent to the first end of the interconnect, the pad array having a first interconnection pad connected to the electrical trace of the conductor layer;

an electrical interface supported by the substrate adjacent to the second end of the interconnect, the electrical interface having a second interconnection pad connected to the electrical trace of the conductor layer,

wherein the conductor layer carries signals between the optical unit and the motherboard.

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